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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/129,675	08/05/1998	ELIYAHOU HARARI	HARI.006USS	4949

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EXAMINER	
TRAN, ANDREW Q	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/129,675	HARARI ET AL.	
	Examiner	Art Unit	
	Andrew Q. Tran	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *63-111* is/are pending in the application.

4a) Of the above claim(s) *92-111* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *63-91* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *see item 6) Other*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: Information Disclosure Statements (IDS) respectively filed on October 30, 2001, September 14, 2005, January 26, 2006 and May 30, 2006.

DETAILED ACTION

Drawings

The drawings are objected to because:

In Fig. 1A, circuit block 31 should be relabeled as --Memory Controller--. In Fig. 1B, circuit block 31 should be relabeled as --Memory Controller Chip--, and circuit block 40 should be relabeled as --Interface Circuit--. In Fig. 2, circuit block 31 should be relabeled as --Memory Controller--. In Fig. 3A, circuit block 233 should be relabeled as --Address Decoder--, and circuit blocks 211 and 213 should be relabeled as --Memory Sector--. In Fig. 3B, signal line 235 should be relabeled as --From Address Decoder--. In Fig. 6, next to reference numeral 31, the legend "Controller" should be relabeled as --Memory Controller--, and circuit block 515 should be relabeled as --REC & S/P--. In Fig. 7, next to reference numeral 31, the legend "Controller" should be relabeled as --Memory Controller--, and circuit block 603 should be relabeled as --INTF IN--. In Fig. 12, circuit block 1081 should be relabeled as --Row Decoder--, and circuit block 1119 should be relabeled as --Erase Decoder--. In Fig. 13, signal line "Serial Out" should be relabeled as --1253-- and should be shown pointing toward circuit block 1150. In Fig. 17A, circuit blocks 1417 and 1415 should be relabeled as --Erase Decoder-- and --Program Decoder--, respectively, and circuit block 1111 should be relabeled as --Internal Address Bus--. Further in Fig. 17A, the "floating gates" should be shown in Master Reference Cell 1400 and Addressed Memory Cell 1420. In Fig. 17B, control gate of transistor 1465 should be relabeled as --CLK K--, and the outputs of circuit block 1480 should be relabeled as --Read Data Bit 1-- to --Read Data Bit L--, respectively. In Fig. 21B, circuit block ΔI_2 should be relabeled as --1543--. And in Fig. 22, memory cells 1 to n should be shown with a "floating gate", as depicted in Fig. 11.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

At page 1, line 10, --now US Pat 5,991,517,-- should be added before "which". At page 6, line 17, "Fig. 2A" should be changed to --Fig. 3A--. At page 6, line 32, "section 2-2" should be changed to --section 10-10--. At page 9, line 7, "system bus 33" should be changed to --system bus 23--. At page 9, line 13, "circuit 55" should be changed to --circuit 57--. At page 12, line 13, "Serial No. 204,175" should be changed to --Serial No. 07/204,175--, and at line 17, "incorporate" should be changed to --incorporated--. At page 13, line 2, "3(9)" should be changed to --4(9)--. At page 13, line 30, "figures 2A and 2B" should be changed to --figures 3A and 3B--. At page 15, line 14, "space" should be changed to --spare--. At page 17, line 23,

"generator 507" should be changed to --generator 503--. At page 19, line 23, "Serial No. 204,175" should be changed to --Serial No. 07/204,175--, and at line 24, "Serial No. 07,337,579" should be changed to --Serial No. 07/337,579--. At page 20, line 8, "data file 516" should be changed to --data file 517--. At page 22, line 8, "Serial No. 204,175" should be changed to --Serial No. 07/204,175--, and at line 10, "Serial No. 07,337,579" should be changed to --Serial No. 07/337,579--. At page 23, line 10, "with" should be changed to --which--. At page 27, line 21, "Serial No. 323,779" should be changed to --Serial No. 07/323,779--, and at line 22, --now US Pat. 5,070,032,-- should be added before "which". At page 28, line 17, "1071" should be changed to --1075--. At page 30, line 10, "address bus 111" should be changed to --address bus 1111--. At page 30, line 28, "Serial No. 204,175" should be changed to --Serial No. 07/204,175--. At page 33, line 5 and 18, "Serial No. 204,175" should be changed to --Serial No. 07/204,175--, respectively. At page 37, line 23, "switches 1525" should be changed to --switches 1521--. At page 39, line 32, "reach" should be changed to --reached--. And at page 43, line 16, "line 1801" should be changed to --line 1809--.

Appropriate correction is required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting

ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 63-91 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 19-24, 26-27 and 36 of U.S. Patent No. 5,991,517. An obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but an examined application claim is not patentably distinct from the reference claim(s) because the examined claim is either anticipated by, or would have been obvious over, the reference claim(s). See e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following :

As to examined claim 63, reference claim 36 recites a nonvolatile semiconductor memory device comprising a memory cell array having a plurality of memory cells, each including a transistor with a charge storage portion (ref clm 36, ln 3-6); a plurality of programming circuits coupled to said memory cell array (i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells, (ii) for selectively applying said write voltages to a part of said memory cells (ref clm 36, ln 7-9); (iii) for determining actual written states of said memory cells (ref clm 36, ln 10-11); and (iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits (ref clm 36, ln 12-13), thereby applying said write voltages only to memory cells which are not sufficiently written to achieve a predetermined written state (ref clm 36, ln 15-18).

As to examined claim 64, see eg. reference claim 36, ln 12-13. As to examined claim 65, "loading data from at least an input line" would be inherently defined in the nonvolatile semiconductor memory device of reference claim 36. As to examined claim 66, see reference claim 36, ln 10. As to examined claim 67, see reference claim 36, ln 12-13. As to examined claims 68 and 69, see reference claim 36, ln 12-18. As to examined claim 70, see reference claim 36, ln 15-18. As to examined claim 71, setting a threshold limit for programming operation would be obvious in the electrically programmable semiconductor memory technology. As to examined claim 72, see reference claim 36, ln 3. As to examined claim 73, it would be obvious to arrange the programming circuits in close proximity to the memory cell array. As to examined claim 74, see reference claim 36, ln 7-9. As to examined claim 75, see reference claim 36, ln 15-18. As to examined claim 76, see reference claim 36, ln 3. As to examined claim 77, see reference claim 36, ln 7-18. As to examined claim 78, see reference claim 36, ln 7-9.

As to examined claims 79-91, by similar analyses as set forth above, these claims are similarly anticipated by, or alternatively obvious over, reference claims 19-24, 26-27 and 36.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 63-91 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al. (JP Kokai 62-188100 with Applicant's Translation submitted in Information Disclosure Statement

filed October 30, 2001, hereafter "Koyama"). See for example, Figs. 1-3 and relevant descriptions thereof.

With regard to claim 63, Koyama discloses a nonvolatile semiconductor memory device comprising a memory cell array wherein each memory cell including a transistor with a charge storage portion (EPROM 1 of Fig. 2); and a plurality of programming circuits (driver/comparator circuits 3_1 - 3_n) coupled to said memory cell array (i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells (flip-flop 7_1 - 7_n, and OR gate 10_1 - 10_n), (ii) for selectively applying said write voltages to a part of said memory cells (gate circuits 4_1 - 4_n), (iii) for determining actual written states of said memory cells (Exclusive OR gate 5_1 - 5_n), and (iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits (Exclusive OR gate 5_1 - 5_n, OR gate 6_1 - 6_n and 10_1 - 10_n, and flip-flop 7_1 - 7_n), thereby applying said write voltages only to memory cells which are not sufficiently written to achieve a predetermined written state.

With regard to claim 64, see driver/comparator circuits 3_1 - 3_n of Fig. 2 and corresponding descriptions. With regard to claim 65, see data inputs 11_1 - 11_n of Fig. 2. With regard to claim 66, the plurality of programming circuits (driver/comparator circuits 3_1 - 3_n) simultaneously determine the actual written states of the memory cells (Exclusive OR gate 5_1 - 5_n) are coupled simultaneously to data bus 2_1 - 2_n . With regard to claim 67, signal lines 10_{1a} - 10_{na} are simultaneously modified in accordance with match/mismatch of write data 10_{1a} - 10_{na} and read data 2_1 - 2_n. With regard to claims 68 and 69, "means for selectively changing voltages of bit lines according data stored in the programming circuits" is inherent from Koyama's teaching to program EPROM 1. With regard to claims 70 and 71, see flowchart of Fig. 1 and description thereof. With regard to claims 72 and 73, see translation, page 12, 3rd

paragraph. With regard to claim 74, see Fig. 2. With regard to claims 75 and 76, see NAND gate 13 in Fig. 2. With regard to claims 77 and 78, see driver/comparator circuits 3_1 - 3_n of Fig. 2, and relevant descriptions thereof.

With regard to claims 79-91, the claim features are similarly matched with Koyama's teachings in a similar fashion, as set forth above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mehrotra et al. (US Pat. 5,172,338) describes read and write circuits and techniques of a multi-state EEPROM.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Q. Tran whose telephone number is (571) 272-1885. The examiner can normally be reached on Mon - Fri 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Q Tran
Primary Examiner
Art Unit 2824

at
July 05, 2006